

**Amendments to the Claims**

**Listing of Claims:**

Original claims 1 – 18 (canceled).

Replacement claims 1 - 17 (canceled).

Claim 19 (new): A semiconductor configuration for controlling a current (I), comprising:

- a) a semiconductor region of a first conductivity type;
- b) an island region of a second conductivity type, opposite said first conductivity type, at least partially buried within the said semiconductor region;
- c) a current path running at least partially within said semiconductor region;
- d) a channel region:
  - d1) forming a part of said semiconductor region,
  - d2) having a basic doping, and
  - d3) including at least one depletion zone for influencing the current;
  - d4) said channel region including a channel conduction region configured for carrying the current, said channel conduction region having the first conductivity type and a higher doping than the basic doping.

Claim 20 (new): The semiconductor configuration according to claim 19, wherein said current path substantially runs in the vertical direction.

Claim 21 (new): The semiconductor configuration according to claim 19, wherein said channel region is formed as a lateral channel region.

Claim 22 (new): The semiconductor configuration according to claim 19 formed as a field effect transistor.

Claim 23 (new): The semiconductor configuration according to claim 19 formed as a junction field effect transistor.

Claim 24 (new): The semiconductor configuration according to claim 19, wherein said semiconductor region is formed of silicon carbide.

Claim 25 (new): The semiconductor configuration according to claim 19, wherein at least 80% of a total charge of said first conductivity type within said channel region is disposed within said channel conduction region.

Claim 26 (new): The semiconductor configuration according to claim 25, wherein at least 90% of a total charge in said channel region is disposed in said channel conduction region.

Claim 27 (new): The semiconductor configuration according to claim 19, which comprises at least one channel compensation region formed in said channel conduction region.

Claim 28 (new): The semiconductor configuration according to claim 27, wherein said at least one channel compensation region has a second conductivity type opposite said first conductivity type.

Claim 29 (new): The semiconductor configuration according to claim 27, wherein said at least one channel compensation region has a higher dopant concentration than said channel conduction region.

Claim 30 (new): The semiconductor configuration according to claim 27, wherein a total charge of said first conductivity type introduced into said channel conduction region is approximately equal in magnitude to a total charge of said second conductivity type introduced into said channel compensation region.

Claim 31 (new): The semiconductor configuration according to claim 27, wherein

said at least one channel compensation region is one of a plurality of channel compensation regions, and wherein a total charge of said first conductivity type in said channel conduction region is approximately equal in magnitude to a total charge of said second conductivity type in all of said channel compensation regions combined.

Claim 32 (new): The semiconductor configuration according to claim 19, wherein said channel region is formed in an epitaxial layer.

Claim 33 (new): The semiconductor configuration according to claim 32, wherein a doping of said epitaxial layer is equal to said basic doping.

Claim 34 (new): The semiconductor configuration according to claim 19, wherein said semiconductor region is formed with two epitaxial layers having a substantially identical doping.

Claim 35 (new): The semiconductor configuration according to claim 19, wherein said semiconductor region is disposed on a substrate of a second conductivity type, opposite said first conductivity type, and said current path runs through said substrate.

Claim 36 (new): The semiconductor configuration according to claim 35, which comprises a shielding region of said first conductivity type disposed between said island region and said semiconductor region, at least on a side of said island region facing said substrate.

Claim 37 (new): A method for producing the semiconductor configuration according to claim 19, the method which comprises the following method steps:

providing a semiconductor substrate;

forming an epitaxial layer with a basic doping on the semiconductor substrate, the epitaxial layer including a channel region, within which a current can be influenced; and

implanting a channel conduction region for carrying current into the epitaxial layer at least in a region of the channel region, the channel conduction region having a higher doping compared with the basic doping.

Claim 38 (new): The method according to claim 37, wherein the epitaxial layer is a first epitaxial layer, and the method further comprises forming a second epitaxial layer, having a doping substantially identical to the basic doping, on the semiconductor substrate, the second epitaxial layer being disposed between the semiconductor substrate and the first epitaxial layer, and wherein the first and second epitaxial layers are applied to the semiconductor substrate progressively and one above the other.